UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,765	12/03/2003	S. Brad Herner	SAND-01158US0	7587

67463 7590 12/31/2007

DUGAN & DUGAN, PC
245 Saw Mill River Road
Suite 309
Hawthorne, NY 10532

EXAMINER	
KIM, JAY C	
ART UNIT	**PAPER NUMBER**
2815	

MAIL DATE	DELIVERY MODE
12/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,765	HERNER, S. BRAD	
	Examiner	Art Unit	
	Jay C. Kim	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-16,18-20,27,28,30-56 and 58-73* is/are pending in the application.

4a) Of the above claim(s) *45-56* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-16,18-20,27,28,30-44 and 58-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed October 9, 2007.

Claim Objections

1. Claim 9 is objected to because of the following informalities: "conductor" on line 2 should be replaced by "conductive". Appropriate correction is required.

2. Claim 11 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. Claim 11 depends on claim 10 and further recites a limitation of "after breakdown of the grown dielectric antifuse layer", which is recited in claim 2 on which claims 10 and 11 depend.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 69-71 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had

possession of the claimed invention. Regarding claim 69, the applicant did not disclose a semiconductor device comprising a silicide layer, a grown dielectric antifuse layer on and in contact with the silicide layer, and a conductive layer comprising titanium nitride on and in contact with the grown dielectric antifuse layer, wherein the electrical connection between the silicide layer and the conductive layer comprising titanium nitride is an electrical connection between portions of a Schottky diode. Claims 70 and 71 depend on claim 69, and therefore claims 70 and 71 contain new matters.

5. Claims 69-71 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Regarding claim 69, Examiner finds it not enabling that an electrical connection between a silicide layer and a conductive layer comprising titanium nitride can be an electrical connection between portions of a Schottky diode. Claims 70 and 71 depend on claim 69, and therefore claims 70 and 71 are not enabling.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 58-64 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 58, Examiner finds it unclear what

"the conductive layer" on line 11 refers to. Claims 59-64 depend on claim 58, and therefore claims 59-64 are also indefinite.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 6, 8, 15, 35, 36 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354).

Regarding claims 2 and 35, Cutter et al. disclose a semiconductor device (Fig. 6B) comprising a silicide layer (642) (col. 8, line 1), a dielectric antifuse layer (610) (col. 8, lines 15-21) on and in contact with the silicide layer (642), and a conductive layer or semiconductor layer (614) (col. 8, lines 24 and 27-28) on and in contact with the dielectric antifuse layer (610), wherein the silicide layer (642) is a refractory metal silicide (col. 8, line 1), and wherein the silicide layer (642) and the dielectric antifuse layer (610) are portions of the semiconductor device (Fig. 6B).

It is inherent that the dielectric antifuse layer has suffered dielectric breakdown, such that an electrical connection exists between the silicide layer and the conductive layer or semiconductor layer.

Cutter et al. differ from the claimed invention by not showing that the dielectric antifuse layer is a grown dielectric antifuse layer and the silicide layer is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, and palladium silicide (claim 2), and that the grown dielectric antifuse layer was grown by oxidizing or nitriding the silicide (claim 35).

Mayer et al. disclose oxidation of silicides (**10.7** Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide (lines 5-7 of **10.7** Oxidation of Silicides).

Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. with the dielectric SiO_2 layer grown by oxidizing a silicide disclosed by Mayer et al. to form an antifuse semiconductor device where a grown SiO_2 dielectric layer is on and in contact with the silicide layer while the rest of the dielectric antifuse layer can be formed by deposition, because the combined semiconductor device would have a grown dielectric SiO_2 layer with less contamination and thus of better quality due to the fact that the SiO_2 layer can be grown right after silicide formation.

Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the silicide layer is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, and palladium silicide.

Kachelmeier discloses a semiconductor device (Fig. 5) comprising a chromium silicide (9) (col. 3, lines 33-38 and 48-53).

Since both Cutter et al. and Kachelmeier teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the refractory metal silicide disclosed by Cutter et al. in view of Mayer et al. can be chromium silicide, because a refractory metal is generally defined as a metal having melting point above 2123 K and the melting point of chromium is 2180 K, and chromium silicide is a well-known electrode material in forming a semiconductor device.

Regarding claim 3, Cutter et al. further disclose that the dielectric antifuse layer (610) comprises silicon oxide (col. 8, lines 17-19).

Regarding claims 6 and 15, Cutter et al. further disclose for the semiconductor device of claim 2 that the conductive layer or semiconductor layer (614) on and in contact with the dielectric antifuse layer (610) may be a metal layer (col. 8, lines 27-28).

Regarding claim 8, Cutter et al. further comprise a first silicon layer (640) (col. 8, line 2), the silicide layer (642) on and in contact with the first silicon layer (640).

Regarding claim 36, Cutter et al. further disclose for the semiconductor device of claim 2 that the silicide layer (642) is in contact with the polysilicon layer (640) (col. 8, line 2).

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the polysilicon layer in contact with the silicide layer is lightly doped or intrinsic, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between a Schottky diode and a conductor.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with an n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor and the semiconductor n- region at the bottom and a conductor at the top, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Regarding claim 40, Cutter et al. further disclose that the silicide (642) is a portion of the Schottky diode (640 and 642 combined).

10. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For

Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) as applied to claim 2 above, and then further in view of Arghavani et al. (US 5,780,346). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Regarding claims 4 and 5, Cutter et al. further disclose for the semiconductor device of claim 2 that the dielectric antifuse layer (610) may comprise a combination of layers (col. 8, lines 21-22), which can be silicon dioxide and silicon nitride (col. 8, lines 17-19).

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the grown dielectric antifuse layer comprises nitrogen (claim 4), and that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride (claim 5).

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15-16) is formed by nitridation of silicon oxide (360) (col. 5, line 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the oxynitride layer grown by nitridation of silicon dioxide disclosed by Arghavani et al. to have the grown dielectric antifuse layer comprise nitrogen, because the combined semiconductor device would

prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) as applied to claim 6 above, and then further in view of Chen (US 2003/0062594). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the grown dielectric antifuse layer is less than about 50 angstroms thick.

Chen discloses a semiconductor device (Fig. 11) comprising a dielectric antifuse layer (60) (line 3 of [0027]) where the bottom oxide layer (57) (line 5 of [0027]) in the dielectric antifuse layer (60) is less than about 50 angstroms thick (lines 7-9 of [0027]).

Since both Cutter et al. and Chen teach a semiconductor device comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the thickness of the silicon dioxide disclosed by Chen, because the combined semiconductor device would be programmed at an intended low voltage by causing dielectric breakdown, while controlling leakage between the silicide layer and the conductive layer.

Further regarding claim 7, the claim is prima facie obvious without showing that the claimed range achieves unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

12. Claims 9-11 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) and then further in view of Choi (US 5,242,851). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Regarding claim 9, Cutter et al. further disclose that the top conductor (614) may comprise polysilicon (col. 8, lines 27-28).

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the conductive or semiconductor layer on and

in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7) and an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14).

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the intrinsic semiconductor layer disclosed by Choi, because the combined semiconductor device would reduce off-state leakage due to the combination of the silicide layer as a bottom electrode and the intrinsic semiconductor layer as a top electrode.

Regarding claims 10 and 11, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode (claim 10), and that the intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer (claim 11).

Choi discloses a programmable interconnect device (Fig. 3P) further comprising an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode, because the intrinsic semiconductor layer will be brought in contact with the silicide layer after breakdown of the grown dielectric antifuse layer.

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi with the Schottky diode structure disclosed by Choi, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Regarding claim 41, Cutter et al. further disclose that the silicide layer (642) is in contact with the polysilicon layer (640) (col. 8, line 2).

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with an n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode formed between the silicide layer as a bottom conductor

and the semiconductor n- region, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Further regarding claim 41, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the conductive layer or semiconductor layer is a portion of a Schottky diode, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7), an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14), and an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.

Since both Cutter et al. and Choi teach a semiconductor memory comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier comprising a Schottky diode between the silicide layer and the bottom semiconductor layer with the Schottky diode formed between the intrinsic semiconductor layer and the top conductor layer disclosed by Choi, because the combined semiconductor device would form a diode device comprising two Schottky diodes in series after programming the antifuse layer.

13. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For

Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier et al. (US 5,897,354) and then further in view of Choi (US 5,242,851) as applied to claim 11 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi are discussed above.

Regarding claims 12-14, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 12), that the memory cell is a portion of a memory array (claim 13), and that the memory array is a monolithic three dimensional memory array (claim 14).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a

diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

14. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) as applied to claim 15 above, and further in view of Cleeves et al. (US 6,541,312). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.

Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode.

Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

15. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) and then further in view of Cleeves et al. (US 6,541,312) as applied to claim 16 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Cleeves et al. are discussed above.

Regarding claims 18-20, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 18), that the memory cell is a portion of a memory array (claim 19), and that the memory array is a monolithic three dimensional memory array (claim 20).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in

view of Cleeves et al. with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

16. Claims 27, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) as applied to claim 6 above, and further in view of Hart et al. (US 5,726,484). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Regarding claim 27, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the conductive layer comprises titanium nitride.

Hart et al. disclose a semiconductor device comprising an antifuse (Fig. 1A) where titanium nitride layer (101) (col. 5, lines 40-44) is deposited on the antifuse layer (105) (col. 5, line 31).

Since both Cutter et al. and Hart et al. disclose a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with

the titanium nitride conductive layer disclosed by Hart et al., because the combined semiconductor device could use titanium nitride against diffusion of copper atoms when copper is used as interconnect material.

Regarding claims 33 and 34, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. differ from the claimed invention by not showing that for a portion of the conductive layer more than about 20 angstroms thick, the density of the titanium nitride is less than about 4.0 grams per cubic cm (claim 33), and that for a portion of the film more than about 20 angstroms thick, the resistivity of the titanium nitride is greater than about 300 microOhm-cms (claim 34).

The claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

17. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) and then further in view of Hart et al. (US 5,726,484) as applied to claim 27 above, and further in view of Cleeves et al. (US 6,541,312). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. are discussed above.

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. differ from the claimed invention by not showing that the conductive layer forms a portion of a Schottky diode.

Cleeves et al. disclose an antifuse stack structure (Fig. 14F) where a lightly doped semiconductor layer (P-) is deposited on a conductor layer (CONDUCTOR), forming a Schottky diode.

Since both Cutter et al. and Cleeves et al. teach a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. with the Schottky diode structure disclosed by Cleeves et al., because the combined semiconductor device would form a diode device after programming the dielectric antifuse layer.

18. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) and then further in view of Hart et al. (US 5,726,484) and then further in view of Cleeves et al. (US 6,541,312) as applied to claim 28 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. and then further in view of Cleeves et al. are discussed above.

Regarding claims 30-32, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. and then further in view of Cleeves et al. differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 30), that the memory cell is a portion of a memory array (claim 31), and that the memory array is a monolithic three dimensional memory array (claim 32).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by

Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Hart et al. and then further in view of Cleeves et al. with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

19. Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) as applied to claim 36 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier are discussed above.

Regarding claims 37-39, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 37), that the memory cell is a portion of a memory array (claim 38), and that the memory array is a monolithic three dimensional memory array (claim 39).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3,

lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

20. Claims 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Kachelmeier (US 5,897,354) and then further in view of Choi (US 5,242,851) as applied to claim 41 above, and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi are discussed above.

Regarding claims 42-44, Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 42), that the

memory cell is a portion of a memory array (claim 43), and that the memory array is a monolithic three dimensional memory array (claim 44).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Kachelmeier and then further in view of Choi with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

21. Claims 58, 59 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851). The teachings of Cutter et al. in view of Mayer et al. are discussed above.

Regarding claim 58, Cutter et al. disclose a semiconductor device (Fig. 6B) comprising a silicide layer (642) (col. 8, line 1), a dielectric antifuse layer (610) (col. 8, lines 15-21) on and in contact with the silicide layer (642), and a conductive layer or semiconductor layer (614) (col. 8, lines 24 and 27-28) on and in contact with the dielectric antifuse layer (610), wherein the silicide layer (642) and the dielectric antifuse layer (610) are portions of the semiconductor device (Fig. 6B).

It is inherent that the dielectric antifuse layer has suffered dielectric breakdown, such that an electrical connection exists between the silicide layer and the semiconductor layer.

Cutter et al. differ from the claimed invention by not showing that the dielectric antifuse layer is a grown dielectric antifuse layer and that a lightly doped or intrinsic semiconductor layer is on and in contact with the grown dielectric antifuse layer.

Mayer et al. disclose oxidation of silicides (**10.7** Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide (lines 5-7 of **10.7** Oxidation of Silicides).

Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. with the dielectric SiO_2 layer grown by oxidizing a silicide disclosed by Mayer et al. to form an antifuse semiconductor device where a grown SiO_2 dielectric layer is on and in contact with the silicide layer while the rest of the dielectric antifuse layer can be formed by deposition, because the combined semiconductor device would have a grown dielectric SiO_2 layer with less contamination

and thus of better quality due to the fact that the SiO_2 layer can be grown right after silicide formation.

Further regarding claim 58, Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that a lightly doped or intrinsic semiconductor layer is on and in contact with the grown dielectric antifuse layer.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7) and an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14).

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the intrinsic semiconductor layer disclosed by Choi, because the combined semiconductor device would reduce off-state leakage due to the combination of the silicide layer as a bottom electrode and the intrinsic semiconductor layer as a top electrode.

Regarding claim 59, Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the intrinsic semiconductor layer forms a portion of a Schottky diode.

Choi further comprises an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode, because the intrinsic semiconductor layer will be brought in contact with the silicide layer after breakdown of the grown dielectric antifuse layer.

Since both Cutter et al. and Choi teach a semiconductor memory comprising a dielectric antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the Schottky diode structure disclosed by Choi, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Regarding claim 65, Cutter et al. disclose a semiconductor device (Fig. 6B) comprising a silicide layer (642) (col. 8, line 1), a dielectric antifuse layer (610) (col. 8, lines 15-21) on and in contact with the silicide layer (642), and a conductive layer or semiconductor layer (614) (col. 8, lines 24 and 27-28) on and in contact with the dielectric antifuse layer (610), wherein the silicide layer (642) and the dielectric antifuse layer (610) are portions of the semiconductor device (Fig. 6B).

It is inherent that the dielectric antifuse layer has suffered dielectric breakdown, such that an electrical connection exists between the silicide layer and the conductive layer or semiconductor layer.

Cutter et al. differ from the claimed invention by not showing that the dielectric antifuse layer is a grown dielectric antifuse layer and that the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Mayer et al. disclose oxidation of silicides (**10.7** Oxidation of Silicides and Fig. 10.19) to grow dielectric SiO_2 on a silicide (lines 5-7 of **10.7** Oxidation of Silicides).

Since both Cutter et al. and Mayer et al. teach a method of fabricating a semiconductor device comprising a silicide layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. with the dielectric SiO_2 layer grown by oxidizing a silicide disclosed by Mayer et al. to form an antifuse semiconductor device where a grown SiO_2 dielectric layer is on and in contact with the silicide layer while the rest of the dielectric antifuse layer can be formed by deposition, because the combined semiconductor device would have a grown dielectric SiO_2 layer with less contamination and thus of better quality due to the fact that the SiO_2 layer can be grown right after silicide formation.

Further regarding claim 65, Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Cutter et al. further disclose that the bottom conductor (112) (col. 1, line 21) of a semiconductor device (Fig. 1) comprising an antifuse layer (110) (col. 1, line 20) is in contact with an n- region (126), forming a Schottky diode.

Since Cutter et al. teach a method of fabricating a semiconductor device comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. with the Schottky diode structure disclosed by Cutter et al. to make a semiconductor device comprising a Schottky diode

formed between the silicide layer as a bottom conductor and the semiconductor n-region, because the combined semiconductor device would form a diode device after programming the antifuse layer.

Further regarding claim 65, Cutter et al. in view of Mayer et al. differ from the claimed invention by not showing that the conductive layer or semiconductor layer is a portion of a Schottky diode, and therefore the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

Choi discloses a programmable interconnect device (Fig. 3P) comprising a dielectric antifuse layer (14) (col. 6, lines 6-7), an intrinsic polysilicon layer (16) (col. 6, line 11) deposited on the dielectric antifuse layer (14), and an aluminum layer (20) (col. 6, line 49) deposited on the intrinsic polysilicon layer (16), forming a Schottky diode.

Since both Cutter et al. and Choi teach a semiconductor memory comprising an antifuse layer, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. comprising a Schottky diode between the silicide layer and the bottom semiconductor layer with the Schottky diode formed between the intrinsic semiconductor layer and the top conductor layer disclosed by Choi, because the combined semiconductor device would form a diode device comprising two Schottky diodes in series after programming the antifuse layer.

22. Claims 60-62 and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851), and further in view of Van Brocklin et al. (US 6,703,652). The teachings of Cutter et al. in view of Mayer et al. and further in view of Choi are discussed above.

Regarding claims 60-62, Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 60), that the memory cell is a portion of a memory array (claim 61), and that the memory array is a monolithic three dimensional memory array (claim 62).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because

the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

Regarding claims 66-68, Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the Schottky diode is a portion of a memory cell (claim 66), that the memory cell is a portion of a memory array (claim 67), and that the memory array is a monolithic three dimensional memory array (claim 68).

Van Brocklin et al. disclose a memory cell (Figs. 1A and 1B) (col. 2, lines 28-29) where an antifuse is a voltage breakdown element (106) (col. 2, lines 38-39) and the memory cell (Figs. 1A and 1B) is a portion of a memory array (Figs. 2A and 2B) (col. 3, lines 40-43), which is a monolithic three dimensional memory array (Fig. 2C) (col. 3, lines 63-65).

Since both Cutter et al. and Van Brocklin et al. teach a method of fabricating a semiconductor memory, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the memory cell and the three dimensional memory array disclosed by Van Brocklin et al. to make a semiconductor device comprising an antifuse layer including a Schottky diode, because the combined semiconductor device would form a diode device after programming the antifuse layer, and could be used in a high density semiconductor memory.

23. Claims 63, 64, 72 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cutter et al. (US 6,323,536) in view of Mayer et al. (Electronic Materials Science: For Integrated Circuits in Si and GaAs, pp. 294-295) and further in view of Choi (US 5,242,851) as applied to claim 63 above, and then further in view of Arghavani et al. (US 5,780,346). The teachings of Cutter et al. in view of Mayer et al. and further in view of Choi are discussed above.

Regarding claims 63 and 64, Cutter et al. further disclose for the semiconductor device of claim 58 that the dielectric antifuse layer (610) may comprise a combination of layers (col. 8, lines 21-22), which can be silicon dioxide and silicon nitride (col. 8, lines 17-19).

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the grown dielectric antifuse comprises nitrogen (claim 63), and that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride (claim 64).

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15-16) is formed by nitridation of silicon oxide (360) (col. 5, line 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the oxynitride layer grown by nitridation of silicon dioxide disclosed by Arghavani et al. to have the grown dielectric antifuse layer

comprise nitrogen, because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

Regarding claims 72 and 73, Cutter et al. further disclose for the semiconductor device of claim 65 that the dielectric antifuse layer (610) may comprise a combination of layers (col. 8, lines 21-22), which can be silicon dioxide and silicon nitride (col. 8, lines 17-19).

Cutter et al. in view of Mayer et al. and further in view of Choi differ from the claimed invention by not showing that the grown dielectric antifuse comprises nitrogen (claim 72), and that the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride (claim 73).

Arghavani et al. disclose a semiconductor device (Fig. 3K) where silicon oxynitride (365 and 366) (col. 6, lines 15-16) is formed by nitridation of silicon oxide (360) (col. 5, line 66 - col. 6, line 2).

Since both Cutter et al. and Arghavani et al. teach a semiconductor device, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor device disclosed by Cutter et al. in view of Mayer et al. and further in view of Choi with the oxynitride layer grown by nitridation of silicon dioxide disclosed by Arghavani et al. to have the grown dielectric antifuse layer comprise nitrogen, because the combined semiconductor device would prevent dopant outdiffusion from the silicide layer or polysilicon layer when polysilicon is used as a semiconductor layer on and in contact with the antifuse layer.

Double Patenting

24. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

25. Claims 2, 3, 9, 11-14, 58 and 60-62 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,853,049. Although the conflicting claims are not identical, they are not patentably distinct from each other because the semiconductor device of claim 2 of current application may comprise a silicide layer, a grown silicon oxide antifuse layer on and in contact with the silicide layer, and a semiconductor layer on and in contact with the grown silicon oxide antifuse layer, which is claimed in claim 1 of U.S. Patent No. 6,853,049.

Response to Arguments

26. Applicant's arguments filed October 9, 2007 have been fully considered but they are not persuasive.

Regarding claim 2, Applicant argues that "claim 2 is patentable, because the silicides recited in claim 2, namely cobalt silicide, platinum silicide, nickel silicide, chromium silicide, and palladium silicide, are not anticipated or rendered obvious by Cutter, which discloses only refractory metal silicides". Chromium is a refractory metal as discussed in the rejection of claim 2, and therefore it would have been obvious that the chromium silicide can be used for the silicide layer disclosed by Cutter et al.

Regarding claim 7, Applicant argues that "dielectric antifuse layer (60) is composed of three layers: bottom oxide layer 57, a silicon nitride layer 58 and a top oxide layer 59", that "layer 57 has a thickness of 10 - 50 angstroms, layer 58 has a thickness of 45 angstroms, and layer 59 has a thickness of 40 - 80 angstroms", and that "the dielectric antifuse layer disclosed in Chen has a minimum thickness of 10 + 45 + 40 = 95 angstroms". As stated in the rejection of claim 7, Examiner used the Chen reference for the thickness of the grown bottom oxide layer, not the deposited layers 58 and 59. Also, Examiner further clarified that the claim 7 is prima facie obvious without showing that the claimed range achieves unexpected results relative to the prior art range, because the thickness of the grown dielectric antifuse layer can be controlled to optimize the programming voltage for the semiconductor device.

Regarding claim 9, Applicant argues that "claim 9 contains the limitation "wherein the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer", that "it is clear that the "conductor or semiconductor layer" is not a dielectric layer which breaks down, but rather is a top conducting layer", that "the intrinsic polysilicon layer of Choi is a dielectric layer which breaks down upon application of a sufficient voltage", that "intrinsic polysilicon layer 21 of Choi (which corresponds to the intrinsic polysilicon layer 16 cited by the Examiner in relation to Fig. 3P) is itself an antifuse layer and not a conductor or electrode layer as interpreted by the Examiner", and that "the cited references therefore do not teach the use of a lightly doped or intrinsic semiconductor layer as a top conductor or semiconductor layer as required by claim 9". Examiner used the Choi reference to show that the top conductive layer or semiconductor layer can be of a multilayer structure similar to the lightly doped or intrinsic semiconductor layer 26 (lines 1-3 of [0050] of current Application) and a heavily doped semiconductor layer 28 (line 3 of [0050] of current Application) in Fig. 3c of current Application. Depending on the voltage applied to the dielectric antifuse layer 14 of Choi, only the dielectric antifuse layer 14 of Choi will break down, inasmuch as only the grown dielectric antifuse layer 24 in Fig. 3c of current Application will break down depending on the voltage applied to the grown dielectric antifuse layer 24. That is, the claim specifies an intended use or field of use.

Regarding claim 41, Applicant argues that "the combination of Cutter et al. in view of Mayer et al. with Choi is improper", because "the antifuse layer of Choi is an

intrinsic polysilicon layer alone or in combination with an oxide layer (col. 6 lines 65 - 68)" and "this intrinsic polysilicon antifuse layer cannot be grown on a silicide as required by Cutter et al. in view of Mayer et al., and by claim 41". As stated above in discussing Applicant's argument regarding claim 9, Examiner used the Choi reference to show that the top conductive layer or semiconductor layer can be of a multilayer structure similar to the lightly doped or intrinsic semiconductor layer 26 and a heavily doped semiconductor layer 28 in Fig. 3c of current Application. Further regarding claim 41, Applicant argues that "the Choi structure cited by the Examiner does not form a Schottky diode", that "once sufficient voltage is applied across the structure, the intrinsic semiconductor layer breaks down, the intrinsic semiconductor layer becomes a conductor layer, and is no longer a semiconductor", that "thus, the post-programming structure is not a diode either", that "after the antifuse layer is broken down, the functional structure would be metal conductor/broken down antifuse conductor/silicide conductor", and that "the broken down antifuse would not form an electrical connection between portions of a Schottky diode, but rather between two conductors". As stated above in discussing Applicant's argument regarding claim 9, depending on the voltage applied to the dielectric antifuse layer 14 of Choi, only the dielectric antifuse layer 14 of Choi will break down, inasmuch as only the grown dielectric antifuse layer 24 in Fig. 3c of current Application will break down depending on the voltage applied to the grown dielectric antifuse layer 24. That is, the claim specifies an intended use or field of use.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay C. Kim whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J. K.
December 26, 2007

Matthew L. Landau
Primary Examiner